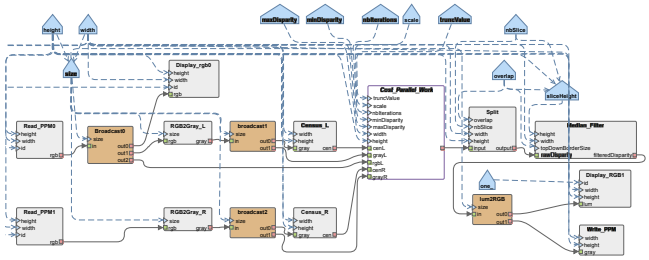
PREESM

PREESM is an **open source rapid prototyping tool**. It simulates signal processing applications and generates code for **heterogeneous multi/many-core embedded systems**. Its dataflow language eases the description of parallel signal processing applications.

Model your Application

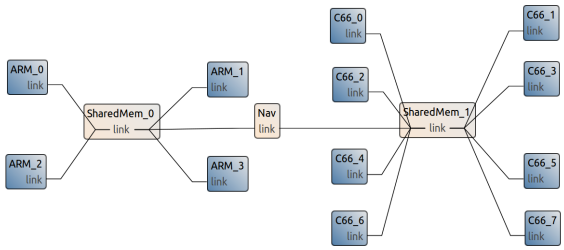
PREESM provides you with a **dataflow language**, designed to **express** easily the **parallelism** of your application and bring out the best of it.



Part of the model of a stereo-matching application

Model your Architecture

PREESM is able to simulate and generate code for a **wide range of embedded systems**. It is particularly aimed to **heterogeneous multi/many-core** systems (e.g., ARMs, DSPs, ASICs).



Model of a Texas Instruments Keystone II board

Prototype your Co-Design

PREESM **simulates the execution** of your parallel application on your architecture. It takes **automatic mapping decisions** and provides you with early information such as **scheduling**, **memory use**, **core loads** and **critical path length**.

This allows you to **compare** different possible soft/hardware **co-designs** to choose the best fit to the system goals and constraints.

Once your co-design chosen, PREESM can **generate parallel code** for your architecture.

Open-Source Software

PREESM is an **open-source** software available on GitHub. It is supported by numerous **tutorials** and a reactive community of programmers and researchers, dedicated to provide you with state of the art **dataflow programming methods and tools**.

http://preesm.sourceforge.net/

https://github.com/preesm/preesm

@PreesmProject

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